REMARKS

Summary of Office Action

Claims 1 and 3 stand rejected under §103(a) as allegedly being unpatentable over Yamaguchi (US 6,329,975) in view of Eto et al. (US 5,301,031).

Claims 2 and 4-5 stand rejected under §103(a) as allegedly being unpatentable over Yamaguchi, Eto et al., and further in view of Sekido et al. (US 5,999,158).

Claims 1 and 3 stand rejected under §103(a) as allegedly being unpatentable over Ueno at al. (US 6,559,839) in view of Eto et al.

Claims 2 and 4-5 stand rejected under §103(a) as allegedly being unpatentable over Ueno at al., Eto et al., and further in view of Sekido et al.

Claims 1 and 3 stand rejected under §103(a) as allegedly being unpatentable over Yoon at al. (US 6,718,478) in view of Eto et al.

Claims 2 and 4-5 stand rejected under §103(a) as allegedly being unpatentable over Yoon at al., Eto et al., and further in view of Sekido et al.

Claim 6 stand allowed.

Summary of Amendment

Claims 1-4 have been amended. Claim 7 stands canceled. No new matter has been added. Claims 1-6 are pending in this application for consideration.

Allowable Claim

Applicant thanks the Examiner for allowance of claim 6. Based on the comments below, Applicant submits that the rest of the pending claims are also in condition for allowance.

All Claims Comply With §103

Claims 1 and 3 stand rejected under §103(a) as allegedly being unpatentable over Yamaguchi, Ueno et al., or Yoon et al., in view of Eto et al. Claims 2 and 4-5 stand rejected under §103(a) as allegedly being unpatentable over Yamaguchi, Ueno et al., or Yoon et al. in combination with Eto et al., and further in view of Sekido et al. Applicant respectfully traverses for the following reasons.

As amended, independent claims 1 and 3 recite, in part, "a source shift clock...the source shift clock being used for sampling and latching the video data by a source driver that applies the video data into data lines formed on a liquid crystal display panel, wherein the source shift clock is reset at said enable initiation time in response to the reset signal irrespective of a change in the number of dot clocks upon conversion of a resolution mode." Support may be found at least on page 10, starting on line 18, of the Substitute Specification, or page 10, starting on line 10 of the originally filed specification. Therefore, no new matter has been added. Applicant submits that Yamaguchi, Ueno et al., Yoon et al., Eto et al., and Sekido et al, whether taken individually or in combination, fail to teach at least these features.

As an initial matter, the rejections in the Office Action are contradictory and confusing at best. The Office alleges that Yamaguchi, Ueno et al., and Yoon et al. teach resetting a source shift clock in each of the rejections. However, the Office also acknowledges that Yamaguchi, Ueno et al., and Yoon et al. all fail to teach a source shift clock (OA: p. 3, 4, and 6) and therefore relies on Eto et al. as teaching a source shift clock. As best understood, Applicant submits that none of the relied-upon references teach resetting a source shift clock.

The Office alleges that Yamaguchi teaches resetting a source shift clock signal (H_{sp}) by applying a reset signal based on a data enable signal to source shift clock 8. (OA: p. 2, §2.) Applicant disagrees.

First, signal H_{sp} is ***not*** a shift clock signal as alleged in the Office Action. It is a ***starting pulse*** selected between a first ***starting pulse*** (H_{sp1}) and a second ***starting pulse*** (H_{sp2}). A starting pulse is not a source shift clock signal. Accordingly, selector 8 is ***not*** a source shift clock. Selector 8 is only a selector circuit that selects between starting pulses (H_{sp1}) and (H_{sp2}) to be output as the starting pulse (H_{sp}) to source driver 3.

Second, the alleged reset signal generated by the data enable signal section circuit 11 (FIG. 4) generates a starting pulse ***select signal*** to be sent to selector 8, 9 to ***select*** one of two starting pulses (H_{sp1}) and (H_{sp2}). The signal generated in FIG. 4 of Yamaguchi is ***not*** a reset signal that resets a source shift clock as alleged in the Office Action.

The Office alleges that Ueno et al. teaches resetting a source shift clock 8 using a reset signal in response to the reset signal generated from counter (7). Applicant disagrees.

The first counter 7 in FIG. 1 of Ueno et al. receives a dot clock signal, data enable signal DENB, and horizontal synchronizing signal H-Sync. By decoding the output of the first counter, the decoder generates a gate drive shift clock signal (CLKV), a course driver shift clock signal (CLKH), and a source driver start pulse signal (STH). Ueno et al. fails to teach that the first counter 7 generates a reset signal that resets a source shift clock as alleged in the Office Action.

The Office alleges that Yoon et al. teaches resetting a source shift clock 60 using a reset signal in response to the reset signal output from the AND2 to start generating a clock signal

(STH) again. Applicant disagrees.

The start pulse signal STH in FIG. 2 of Yoon et al. is not a source shift clock signal as alleged in the Office Action. As discussed above, a start pulse signal is ***not*** a source shift clock signal. Accordingly, D flip-flop 60 is ***not*** a source shift clock. Therefore, neither the source shift clock reset unit 50 nor the AND2 gate signal resets a source shift clock as alleged in the Office Action.

The Office alleges that Eto et al. teaches a source shift clock. Applicant disagrees. As explained before and reasserted here, Eto et al. also fails to teach a source shift clock.

The Office continues to allege that the scanning circuit 7 of Eto et al. is a source shift clock, citing to FIGs. 1-2 and column 3, lines 1-50 and column 4, lines 4-12. As explained before and reasserted here, scanning circuit 7 of Eto et al. is not a source shift clock. FIG. 1 of Eto et al. shows that scanning circuit 7 includes a horizontal shift register 14 that scans in video data (9) and a sample-and-hold circuit 15 that latches the video data scanned into the horizontal shift register 14 to apply the video data to the data lines 16-1 to 16-n. At best, Eto et al. mentions that the horizontal shift register 14 uses a horizontal shift register shift clock signal CKH (col. 4, ll. 8-9). However, Eto et al. fails to teach a source shift clock or resetting the source shift clock as alleged in the Office Action.

Moreover, as amended, independent claims 1 and 3 recite, in part, "a source shift clock...the source shift clock being used for sampling and latching the video data by a source driver that applies the video data into data lines formed on a liquid crystal display panel; wherein the source shift clock is reset at said enable initiation time in response to the reset signal

irrespective of a change in the number of dot clocks upon conversion of a resolution mode." Yamaguchi, Ueno et al., Yoon et al., Eto et al., and Sekido et al, whether taken individually or in combination, fail to teach at least these features. Accordingly, Applicant respectfully requests that the §103 rejections of claims 1 and 3 be withdrawn.

Claims 2, 4, and 5 each depends respectively from one of claims 1 and 3, thereby incorporating all the features of their respective base claims. Accordingly, Applicant respectfully submits that claims 2, 4 and 5 are each allowable over Yamaguchi, Ueno et al., Yoon et al., Eto et al., and Sekido et al, whether taken individually or in combination, for at least the reasons presented above. Therefore, Applicant respectfully requests that the §103 rejections to claims 2, 4, and 5 be withdrawn.

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CONCLUSION

In view of the foregoing, reconsideration and timely allowance of the pending claims are respectfully requested. Should the Examiner feel that there are any issues outstanding after consideration of the response, the Examiner is invited to contact the Applicant's undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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